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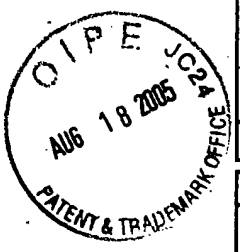

Effective on 12/08/2004.
Fees pursuant to the Consolidated Appropriations Act, 2005 (H.R. 4818).

FEE TRANSMITTAL
For FY 2005

☐ Applicant claims small entity status. See 37 CFR 1.27

TOTAL AMOUNT OF PAYMENT ($) 910.00

Complete if Known	
Application Number	10/643,375
Filing Date	August 18, 2003
First Named Inventor	Chien-Ping Huang
Examiner Name	D. W. Owens
Art Unit	2811
Attorney Docket No.	59744 (71987)

METHOD OF PAYMENT (check all that apply)

☐ Check ☐ Credit Card ☐ Money Order ☐ None ☐ Other (please identify): _____

☒ Deposit Account Deposit Account Number: 04-1105 Deposit Account Name: Edwards & Angell, LLP

For the above-identified deposit account, the Director is hereby authorized to: (check all that apply)

☒ Charge fee(s) indicated below ☐ Charge fee(s) indicated below, **except for the filing fee**

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FEE CALCULATION

1. BASIC FILING, SEARCH, AND EXAMINATION FEES

	FILING FEES		SEARCH FEES		EXAMINATION FEES		
Application Type	**Fee ($)**	**Small Entity Fee ($)**	**Fee ($)**	**Small Entity Fee ($)**	**Fee ($)**	**Small Entity Fee ($)**	**Fees Paid ($)**
Utility	300	150	500	250	200	100	
Design	200	100	100	50	130	65	
Plant	200	100	300	150	160	80	
Reissue	300	150	500	250	600	300	
Provisional	200	100	0	0	0	0	

2. EXCESS CLAIM FEES

Fee Description	Fee ($)	Small Entity Fee ($)
Each claim over 20 (including Reissues)	50	25
Each independent claim over 3 (including Reissues)	200	100
Multiple dependent claims	360	180

Total Claims		Extra Claims	Fee ($)		Fee Paid ($)
_____	- 20 =	_____	x _____	=	_____

Indep. Claims		Extra Claims	Fee ($)		Fee Paid ($)
_____	- 3 =	_____	x _____	=	_____

Multiple Dependent Claims	
Fee ($)	**Fee Paid ($)**
_____	_____

3. APPLICATION SIZE FEE

If the specification and drawings exceed 100 sheets of paper (excluding electronically filed sequence or computer listings under 37 CFR 1.52(e)), the application size fee due is $250 ($125 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).

Total Sheets		Extra Sheets		Number of each additional 50 or fraction thereof		Fee ($)		Fee Paid ($)
_____	- 100 =	_____	/50	_____	(round up to a whole number) x	_____	=	_____

4. OTHER FEE(S)

	Fees Paid ($)
Non-English Specification, $130 fee (no small entity discount)	
Other (e.g., late filing surcharge): 1251 Extension for response within first month	120.00
1801 Request for continued examination (RCE) (see 37 ...	790.00

SUBMITTED BY					
Signature		Registration No. (Attorney/Agent)	42,693	Telephone	(617) 439-4444
Name (Print/Type)	Steven M. Jensen			Date	August 18, 2005

I hereby certify that this correspondence is being deposited with the U.S. Postal Service as Express Mail, Airbill No. EV711310753US, in an envelope addressed to: MS RCE, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on the date shown below.

Dated: August 18, 2005 Signature: Michelle Chicos (Michelle Chicos)

504384

Docket No. 59744 (71987)

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICANT:	C. Huang et al.		
U.S. SERIAL NO:	10/643,375	EXAMINER:	D. Owens
FILED:	August 18, 2003	GROUP:	2811
FOR:	SEMICONDUCTOR PACKAGE HAVING CONDUCTIVE BUMPS ON CHIP AND METHOD FOR FABRICATING THE SAME		

CERTIFICATE OF FACSIMILE TRANSMISSION

I hereby certify that this paper (along with any paper referred to as being attached or enclosed) is being transmitted by facsimile to the U.S. Patent & Trademark Office by facsimile number 571-273-8300 on July 18, 2005.

By _____
Steven M. Jensen

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

AMENDMENT

Applicants are in receipt of the Office Action dated April 18, 2005 of the above-referenced application. Please amend the application as follows:

Amendments to the claims are reflected in the listing of claims which begins on page 2 of this paper.

Remarks begin on page 7 of this paper.

Amendments to the claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of claims:

Claim 1 (currently amended): A semiconductor package having conductive bumps on a chip, comprising:

at least one chip having an active surface and an opposite inactive surface, and having a plurality of bond pads formed on the active surface;

a plurality of conductive bumps respectively formed on the bond pads of the chip;

~~an~~ a single encapsulation body for completely encapsulating the chip and the conductive bumps, wherein ends of the conductive bumps are exposed outside of the encapsulation body and flush with a surface of the encapsulation body;

a plurality of first conductive traces formed ~~on~~ at the surface of the encapsulation body exposing the conductive bumps and electrically connected to the exposed ends of the conductive bumps;

a solder mask layer applied over the first conductive traces and having a plurality of openings for exposing predetermined portions of the first conductive traces; and

a plurality of solder balls respectively formed on the exposed portions of the first conductive traces.

Claim 2 (original): The semiconductor package of claim 1, further comprising: at least one dielectric layer and a plurality of second conductive traces formed on the dielectric layer, the dielectric layer and the second conductive traces interposed between the first conductive traces and the solder mask layer, wherein the dielectric layer is located on the first conductive traces and has a plurality of vias by which the predetermined portions of the first conductive traces are exposed and electrically connected to the second conductive traces, and the solder mask layer is located on the second conductive traces whose predetermined portions are exposed via the openings of the solder mask layer and respectively connected to the plurality of solder balls.

Claim 3 (original): The semiconductor package of claim 1, wherein the inactive surface of the chip is exposed outside of the encapsulation body.

Claim 4 (original): The semiconductor package of claim 2, wherein the inactive surface of the chip is exposed outside of the encapsulation body.

Claim 5 (original): The semiconductor package of claim 1, wherein the conductive bump is selected from the group consisting of solder bump, high lead solder bump, gold bump, and gold stud bump.

Claim 6 (original): The semiconductor package of claim 2 wherein the conductive bump is selected from the group consisting of solder bump, high lead solder bump, gold bump, and gold stud bump.

Claim 7 (original): The semiconductor package of claim 1, wherein the exposed portions of the first conductive traces are terminals.

Claim 8 (original): The semiconductor package of claim 2, wherein the exposed portions of the second conductive traces are terminals.

Claim 9 (withdrawn): A method for fabricating a semiconductor package having conductive bumps on a chip, comprising the steps of:

preparing a wafer comprising a plurality of chips, each chip having an active surface and an opposite inactive surface, and having a plurality of bond pads formed on the active surface;

forming a plurality of conductive bumps respectively on the bond pads of each of the chips;

singulating the wafer to separate the plurality of chips, each chip having a plurality of the conductive bumps thereon; providing a carrier for accommodating the plurality of chips, and mounting the conductive bumps of each of the chips on a surface of the carrier;

forming an encapsulation body on the surface of the carrier for encapsulating the chips and the conductive bumps;

removing the carrier to allow ends of the conductive bumps to be exposed outside of the encapsulation body and flush with a surface of the encapsulation body;

forming a plurality of conductive traces on the surface of the encapsulation body and electrically connecting the conductive traces to the exposed ends of the conductive bumps;

applying a solder mask layer over the conductive traces and forming a plurality of openings through the solder mask layer for exposing predetermined portions of the conductive traces;

depositing a plurality of solder balls respectively on the exposed portions of the conductive traces; and

cutting the encapsulation body to form a plurality of individual semiconductor packages each having at least one of the singulated chips.

Claim 10 (withdrawn): The method of claim 9, further comprising a step of: prior to forming the plurality of conductive traces, performing a grinding process to grind the surface of the encapsulation body flush with the ends of the conductive bumps.

Claim 11 (withdrawn): The method of claim 9, further comprising a step of: prior to forming the plurality of conductive traces, performing a grinding process to grind the surface of the encapsulation body flush with the ends of the conductive bumps, and grind off a portion of the encapsulation body covering the inactive surfaces of the chips to expose the inactive surfaces.

Claim 12 (withdrawn): The method of claim 9, wherein the conductive bump is selected from the group consisting of solder bump, high lead solder bump, gold bump, and gold stud bump.

Claim 13 (withdrawn): The method of claim 9, wherein the exposed portions of the conductive traces are terminals.

Claim 14 (withdrawn): The method of claim 9, wherein the carrier is a tape.

Claim 15 (withdrawn): A method for fabricating a semiconductor package having conductive bumps on a chip, comprising the steps of:

preparing a wafer comprising a plurality of chips, each chip having an active surface and an opposite inactive surface, and having a plurality of bond pads formed on the active surface;

forming a plurality of conductive bumps respectively on the bond pads of each of the chips;

singulating the wafer to separate the plurality of chips, each chip having a plurality of the conductive bumps thereon;

providing a carrier for accommodating the plurality of chips, and mounting the conductive bumps of each of the chips on a surface of the carrier;

forming an encapsulation body on the surface of the carrier for encapsulating the chips and the conductive bumps;

removing the carrier to allow ends of the conductive bumps to be exposed outside of the encapsulation body and flush with a surface of the encapsulation body;

forming a plurality of first conductive traces on the surface of the encapsulation body and electrically connecting the first conductive traces to the exposed ends of the conductive bumps;

coating at least one dielectric layer on the first conductive traces and forming a plurality of vias through the dielectric layer for exposing predetermined portions of the first conductive traces;

forming a plurality of second conductive traces on the dielectric layer and electrically connecting the second conductive traces to the exposed portions of the first conductive traces;

applying a solder mask layer over the second conductive traces and forming a plurality of openings through the solder mask layer for exposing predetermined portions of the second conductive traces;

depositing a plurality of solder balls respectively on the exposed portions of the second conductive traces; and

cutting the encapsulation body to form a plurality of individual semiconductor packages each having at least one of the singulated chips.

Claim 16 (withdrawn): The method of claim 15, further comprising a step of: prior to forming the first conductive traces, performing a grinding process to grind the surface of the encapsulation body flush with the ends of the conductive bumps.

Claim 17 (withdrawn): The method of claim 15, further comprising a step of: prior to forming the first conductive traces, performing a grinding process to grind the surface of the encapsulation body flush with the ends of the conductive bumps, and grind off a portion of the encapsulation body covering the inactive surfaces of the chips to expose the inactive surfaces.

Claim 18 (withdrawn): The method of claim 15, wherein the conductive bump is selected from the group consisting of solder bump, high lead solder bump, gold bump, and gold stud bump.

Claim 19 (withdrawn): The method of claim 15, wherein the exposed portions of the second conductive traces are terminals.

Claim 20 (withdrawn): The method of claim 15, wherein the carrier is a tape.

REMARKS

Claims 1-20 are pending in the application. Claims 9-20 were withdrawn from consideration as being drawn to non-elected subject matter. Claim 1 has been amended by the present amendment. The amendment is fully supported by the application as originally filed (see, e.g., page 8, last paragraph to page 9, first paragraph; FIGS. 1 and 2C).

As amended, claim 1 recites a semiconductor package in which a chip and conductive bumps are completely encapsulated by a **single** encapsulation body, and a plurality of conductive traces are formed at the surface of the encapsulation body exposing the conductive bumps, the conductive traces being electrically connected to exposed ends of the conductive bumps.

For example, referring to FIGS. 1 and 2C, the encapsulation body 22 completely encapsulates the chip 20 and conductive bumps 21. In other words, the encapsulation body 22 is a **single** encapsulation body for encapsulating all of the chips 20 and conductive bumps 21 (see page 8, last paragraph to page 9, first paragraph). As shown in FIG. 1, conductive traces 23 are formed at the surface of the encapsulation body on exposed ends of the conductive bumps 21.

Claims 1, 2, and 5-8 were rejected under 35 USC 102(e) as being anticipated by U.S. Patent 6,701,614 to Ding et al. ("Ding"). Claims 3 and 4 were rejected under 35 USC 103(a) as being unpatentable over Ding in view of U.S. Patent 6,734,534 to Vu et al. ("Vu"). These rejections are respectfully traversed.

Ding does not teach or suggest a semiconductor package in which a chip and conductive bumps are completely encapsulated by a **single** encapsulation body, and a plurality of conductive traces are formed at the surface of the encapsulation body exposing the conductive bumps, as recited in claim 1.

Referring to FIG. 4h of Ding, as cited in the Final Office Action, die 30 is encapsulated by an encapsulating material 40 (see column 5, lines 53-55). A first dielectric layer 61 is formed on a surface of the encapsulating material 40 (see column 5, lines 57-59).

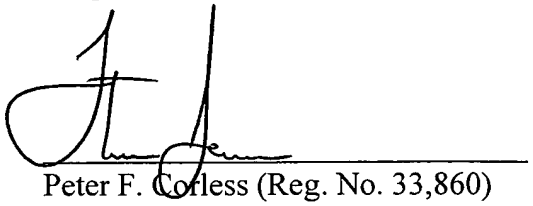
In the Final Office Action, the encapsulating material 40 and the first dielectric layer 61 of Ding were cited as corresponding to Applicants' claimed "encapsulation body."

However, the encapsulating material 40 and first dielectric layer 61 do not constitute a **single** encapsulation body for completely encapsulating a chip and conductive bumps. Moreover, in Ding, the conductive traces 72 are formed on the first dielectric layer 61, not at the surface of an encapsulation body exposing the conductive bumps.

For at least the reasons discussed above, the Ding reference does not anticipate or otherwise render obvious the Applicants' claimed invention.

It is believed the application is in condition for immediate allowance, which action is earnestly solicited.

Respectfully submitted,



Date: July 18, 2005

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